

## A 10 GHz Quasi-Optical Grid Amplifier Using Integrated HBT Differential Pairs

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We report the fabrication and testing of a 10 GHz grid amplifier utilizing sixteen GaAs chips each containing an HBT differential pair plus integral bias/feedback resistors. The overall amplifier consists of a 4x4 array of unit cells on an RT Duroid™ board having a relative permittivity of 2.2. Each unit cell consists of an emitter-coupled differential pair at the center, an input antenna which extends horizontally in both directions from the two base leads, an output antenna which extends vertically in both directions from the two collector leads, and high inductance bias lines. In operation, the active grid array is placed between a pair of crossed polarizers. The horizontally polarized input wave passes through the input polarizer and couples to the input leads. An amplified current then flows on the vertical leads, which radiate a vertically polarized amplified signal through the output polarizer. The polarizers serve dual functions, providing both input-output isolation as well as independent impedance matching for the input and output ports. The grid thus functions essentially as a free-space beam amplifier. Calculations indicate that output powers of several watts per square centimeter of grid area should be attainable with optimized structures.

Quasi-optical grid devices including oscillators, multipliers, mixers, and beam steerers have already been demonstrated [1,2,3,4]. Motivation for studying quasi-optical devices is two-fold: free-space power combining is more efficient at high frequencies than power combining in guided wave structures, and transmitting and receiving systems based on monolithic implementations of quasi-optical elements have the potential for being smaller, lighter, and substantially less costly than conventional phased-array systems.

The AlGaAs/GaAs HBT material was grown by MBE.

LAYER	THICKNESS (μm)	TYPE	DOPING (cm <sup>-3</sup> )	AlAs FRACTION
Cap	0.16	n <sup>+</sup>	5x10 <sup>18</sup>	0
Emitter	0.1	n	0.5-1.5x10 <sup>18</sup>	0 - .25 - 0
Base	0.07	p <sup>+</sup>	0.5 - 1.0x10 <sup>20</sup>	0
Collector	0.7	n	3 - 6x10 <sup>16</sup>	0
Subcollector	0.6	n <sup>+</sup>	6x10 <sup>18</sup>	0

The devices are implant isolated and have an active emitter area of 40 square microns. The transistors exhibit  $f_T = 65$  GHz, and  $f_{max} = 90$  GHz. Each chip contains a differential pair with 1.7kΩ collector-base feedback resistors and a 250Ω emitter bias resistor which also serves to suppress common mode gain.

The amplifier exhibits a peak gain of 12dB at 9.9 GHz, with a 3dB bandwidth which extends from 9.55 GHz to 10.3 GHz. The peak gain and bandwidth are sensitive to polarizer position, indicating that the polarizers provide good matching to free space (as a reference point, the transistors have 18dB unilateral gain at 10 GHz). Output power is linear with input power, indicating that the grid operates as an amplifier rather than as an injection-locked oscillator. Gain saturation can be observed at low dc bias and high input rf levels.

This amplifier represents a significant advance over the previously reported grid amplifier [5] beyond its higher operating frequency, larger gain, and wider bandwidth. Where the previous grid required both front and backside wiring on the substrate (which would be cumbersome in a monolithic implementation), this amplifier utilizes frontside wiring only. Where the previous amplifier utilized packaged discrete MESFETs, in this amplifier the contents of each unit cell are monolithically integrated with the exception of the metal lines which make up the antenna array. This amplifier therefore represents a substantial step toward monolithic integration of an entire grid, which will be required for higher frequency operation and low cost.

#### References

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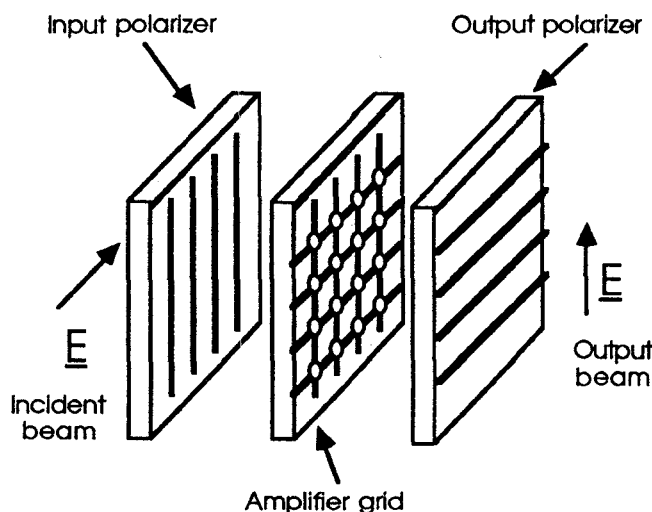


Figure 1: Perspective view of Grid Amplifier. Horizontally polarized input wave is incident from the left; vertically polarized output wave is radiated to the right. The polarizers consist of parallel copper lines on Duroid boards

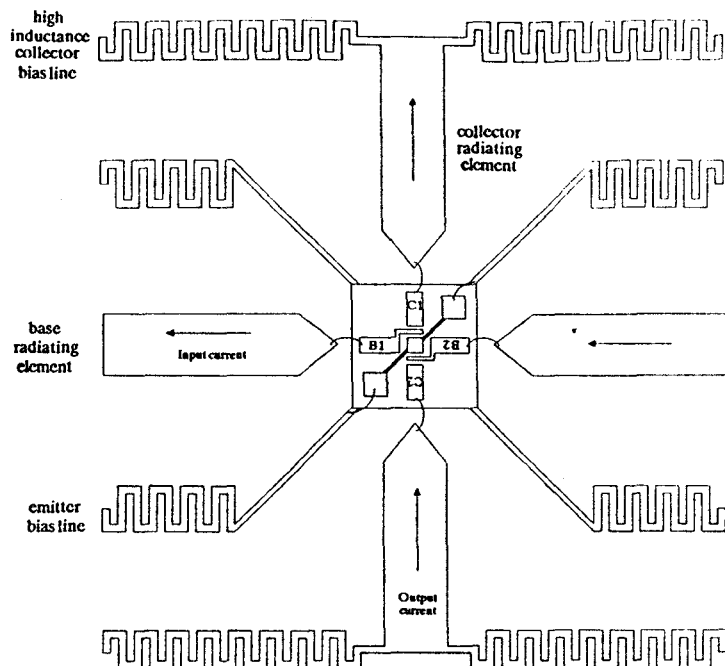


Figure 2: Plan view of unit cell. These cells are periodically repeated in a two dimensional array. The HBT differential pair chips are bonded to the centers of the antenna patterns which are etched into a copper clad Duroid board. Note that the emitter bias lines are joined beneath the chip.

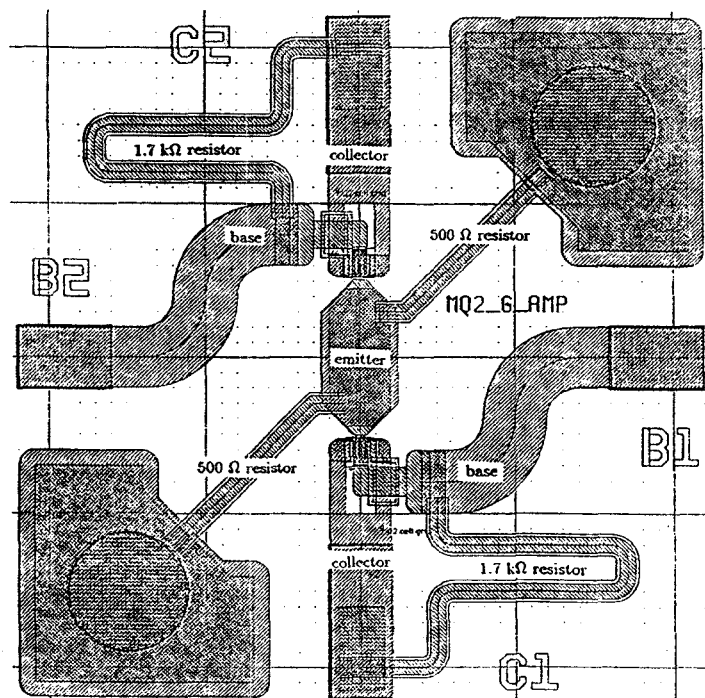


Figure 3: Plan view of the Rockwell differential pair HBT chip. The 250Ω emitter bias resistor is implemented as a parallel combination of two 500Ω resistors for symmetry reasons.

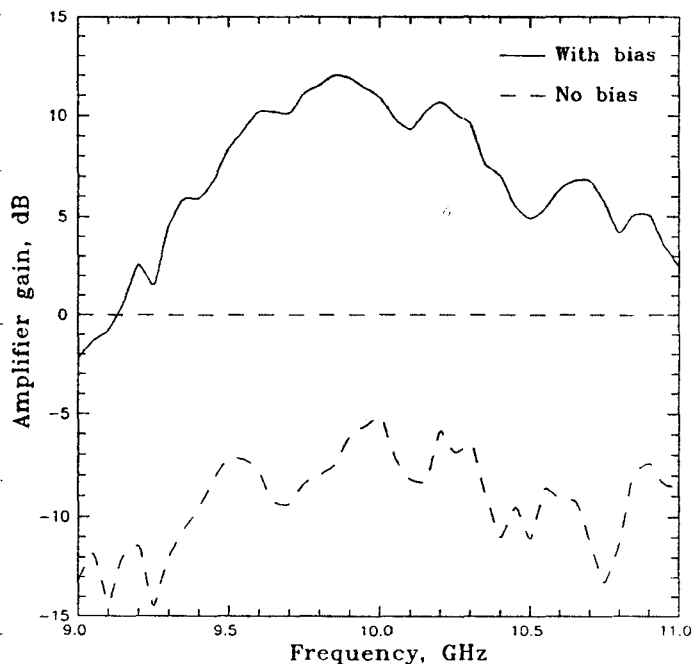


Figure 4: Gain versus frequency plot for Grid Amplifier. Output power is proportional to input power for the entire dynamic range of our measurement apparatus (>30dB) with 5V bias supplied to the grid. At 2.5V bias, grid can be saturated at high rf input power.